REMARKS

Claims 1-55 are pending in the application.

Claims 5-9, 13-17, and 20-34 stand rejected.

Claims 4, 9, 10, 38, and 48 have been amended. These amendments do not introduce new matter. The amendments to claims 4 and 10 correct typographical errors. The amendments to claims 9 and 38 are discussed below. Support for the amendment to claim 48 can be found on line 37 of page 32 of the specification.

Claim 55 has been added. Support for claim 55 can be found on line 37 of page 32 of the specification.

Formal Matters

The "Cross-Reference to Related Applications" section of the specification has been amended to remove the client reference numbers and to add the filing dates and serial numbers of the related applications.

The "Brief Description of the Drawings" section of the specification has been amended to include a brief description of Figures 12 and 13. Support for this amendment can be found on line 26 of page 33 and line 32 of page 35. No new matter has been added by this amendment.

Objection to the Specification

The Abstract has been amended to include no more than 150 words, as specified in 37 C.F.R. §1.72. Accordingly, Applicant believes that this objection has been overcome.

Objection to the Claims

Claim 4 has been amended to include proper punctuation. Accordingly, Applicant believes that this objection has been overcome.

Rejection of Claims under 35 U.S.C. §112

Claims 9 and 38 stand rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. These claims have been amended to explicitly define d0-d2 and q0-q2. Support for the amendments can be found, at least, on page 8 of the specification.

Additionally, the equations in the claims as well as the specification have been amended to correct a typographical error, thus making it clear that each of the minimal degree equations σ^i (i = 1-3) is a function of the variable X (e.g., as shown on pages 34-35 of the specification), as is readily apparent by virtue of X being included on the right hand side of several of the equations. This is further evidenced by reference to pages 155-159 and 167-169 of "Error Control Coding: Fundamentals and Applications," by Shu Lin and Daniel J. Costello (incorporated by reference in the present application on p. 6 of the specification), which describe these minimal polynomials as being functions of X. Accordingly, Applicants believe that the §112 rejections have been overcome with respect to the amended claims.

Rejection of Claims under 35 U.S.C. §102

Claims 1, 5, 9, 10, 11, 12, 25, 30, 31, and 32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Shen et al (U.S. Pat. No. 6,199,188) (hereinafter referred to as "Shen"). Applicant respectfully traverses this rejection.

The cited art fails to anticipate, teach, or suggest: "extracting an error polynomial from the data signal based on no more than six equations having no more than two branch decisions," as recited in claim 1. The cited portions of Shen are concerned with locating errors within a code word by finding the roots of an error locator polynomial (e.g., see Shen, Abstract and col. 7). With respect to actually generating the error locator polynomial itself, Shen teaches that "the syndrome generator sends the syndromes to an error locator polynomial generator 14, which produces in a conventional manner from the syndromes an error locator polynomial of degree 'e', where e is the number of errors in the code word." Shen does not further elaborate on the "conventional manner" in which the error locator polynomial is produced, and thus Shen clearly

fails to anticipate, teach, or suggest generating an "error polynomial" in the manner recited in claim 1. Claims 5, 9, 10, 11, and 12 are patentable over the cited art for similar reasons.

The cited art also fails to teach or suggest a system that includes "a plurality of Galois field multiply accumulators; and means for using said Galois field multiply accumulators to generate an error polynomial based on values provided at said syndrome inputs, by executing no more than six equations with two branch decisions," as recited in claim 25. The Examiner cites FIG. 4 of Shen as anticipating the Galois field multiply accumulators of claim 25. Office Action, p. 4. FIG. 4 shows a "subsystem 400 [that] determines the cubic root of an element β in $GF(2^{m+1})$ by raising that element to the power u in multipliers 402, which include of one or more conventional Galois Field multipliers." Shen, col. 12, lines 30-33. The cubic root of the element β is calculated as part of the process of determining the location of errors, which is in turn based on an error locator polynomial which is "produce[d] in a conventional manner from the syndromes." Shen, col. 4, lines 40-45, col. 4, line 66 - col. 5, line 8. Thus, the Galois field multipliers of FIG. 4, which are used to raise an element to the power u, clearly neither teach nor suggest using Galois field multiply accumulators to generate an error polynomial, as recited in claim 25. No other cited portion of Shen, either alone or in combination with FIG. 4, teaches or suggests this feature. Instead, the other cited portions of Shen simply describe that an error polynomial can be generated from syndromes (col. 1, lines 53-55), and that "for any degree-three error locator polynomial, $\sigma(x)$, the system determines error locations" (Shen, col. 7, lines 9-10) according to the methodology described in col. 7. Applicant notes that col. 7 is concerned with determining error locations, based on an error locator polynomial, rather than with generating an error locator polynomial itself. Accordingly, the cited art clearly fails to teach or suggest "using said Galois field multiply accumulators to generate an error polynomial based on values provided at said syndrome inputs, by executing no more than six equations with two branch decisions," as recited in claim 25. Claims 30-32 are patentable over the cited art for similar reasons.

Rejection of Claims under 35 U.S.C. §103

Claims 2-4, 6, 13, 14, 18, 24, 26, 38, 39, and 42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen in view of Oh et al (U.S. Pat. No. 5,583,499) (hereinafter referred to as "Oh"). Applicants respectfully traverse this rejection.

Claims 2-4 and 6 are patentable by virtue of their dependence upon allowable claim 1. Claim 26 is patentable by virtue of its dependence upon allowable claim 25.

Further with respect to claim 3, Shen and Oh, both alone or in combination, fail to teach or suggest "extracting an error polynomial from the data signal based on no more than six equations having no more than two branch decisions", wherein "said extracting step includes the step of controlling a plurality of Galois field multiply accumulators using a state machine," as recited in claim 3. In particular, neither Oh nor Shen teach or suggest the use of state machines and Galois field multiply accumulators to extract an error polynomial.

With respect to claim 13, the cited art fails to teach or suggest calculating a plurality of minimum-degree polynomials associated with the BCH code, using the Galois field multiply accumulators; and generating an error polynomial based on the minimum-degree polynomials, said calculating and generating steps extracting the error polynomial in no more than 12 clock cycles. In particular, neither Shen nor Oh teaches or suggests using Galois field multiply accumulators to calculating a plurality of minimum-degree polynomials, which are then used to generate an error polynomial. As noted above, Shen teaches simply that an error polynomial can be generated using conventional means. Oh teaches a system that uses an iterative process to calculate an error locator polynomial. Oh states that "an apparatus 1 for updating the error locator polynomial in accordance with the present invention... includes two multiplication blocks 10 and 30, and an addition block 60." Oh, col. 5, lines 58-62. This apparatus is not a Galois field multiply accumulator, as recited in claim 13. Accordingly, Oh, both alone and in combination with Shen, fails to teach or suggest calculating a plurality of minimum-degree polynomials associated with the BCH code, using Galois field multiply accumulators. For at least this reason, claim 13 is patentable over the cited art. Claims 14, 18, and 24 are patentable over the cited art for at least the foregoing reasons provided with respect to claim 13.

With respect to claim 38, the cited art fails to teach or suggest a plurality of Galois field multiply accumulators and a state machine programmed to use said Galois field multiply accumulators to generate an error polynomial based on the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(X) = 1 + S_1X$,

(4) if $(d_1 = 0)$ then $\sigma^2(x) = \sigma^1(x)$

else if $(d_0 = 0)$ then $\sigma^2(X) = q_0\sigma^1(X) + d_1X^3$

else $\sigma^2(X) = q_0\sigma^1(X) + d_1X^2$,

(5) $d_2 = S_5\sigma_0 + S_4\sigma_1 + S_3\sigma_2 + S_2\sigma_3$, and

(6) if $(d_2 = 0)$ then $\sigma^3(X) = \sigma^2(X)$

else $\sigma^3(X) = q_1\sigma^1(X) + d_1X^3$,

where S_i are error syndromes, σ^i are minimum-degree polynomials, σ_i are four coefficients for $\sigma^2(X)$, d_0-d_2 are correction factors, q_0-q_1 are additional correction factors, q_0 is equal to d_0 unless d_0 is zero, when q_0 is 1, and q_1 is equal to d_1 unless d_1 is zero, when $q_1 = q_0$.

The Examiner cites col. 7, line 7 - col. 8, line 3 of Shen as teaching the equations used to generate the error polynomial. The cited portion of Shen is concerned with determining error locations for any degree-three error locator polynomial by solving: $\sigma(x) = \sigma_3x^3 + \sigma_2x^2 + \sigma_1x + \sigma_0 = 0$. Shen, col. 7, lines 7-11. Thus, the cited portion of Shen is not directed to generating an error polynomial. Instead, the cited portion of Shen is directed to determining error locations for a degree-three error locator polynomial, which has already been calculated. As noted above, Shen simply teaches that the error locator polynomial is generated in a "conventional manner" from the syndromes. Applicant further notes that, while the cited portion of Shen does include a number of equations, none of the equations appear to be equivalent to the equations recited in claim 38. For example, unlike the equations in claim 38, none of the equations in Shen depend upon any of the syndromes S_1-S_5. Thus, for at least these reasons, claim 38 is patentable over the cited art. Claims 39 and 42 are patentable over the cited art for at least the foregoing reasons provided above with respect to claim 38.

Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen in further view of Erhart et al (U.S. Pat. No. 5,051,999). The rejection relies on the same rationale as the 102(e) rejection of claim 1. Accordingly, claim 7 is patentable over the cited art for at least the reasons provided above with respect to claim 1. Furthermore, Erhart, either alone or in combination with Shen, does not teach or suggest "extracting an error polynomial from the data signal based on no more than six equations having no more than two branch decisions," as recited in claim 1.

Claims 8, 27-29, and 33-37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen in view of Stenerson (U.S. Pat. No. 4,597,083) (hereinafter referred to as "Stenerson"). Claim 8 is patentable over the cited art for reasons similar to those provided above with respect to claim 1. Claims 27-29 and 33-27 are patentable over the cited art for reasons similar to those provided above with respect to claim 25.

Claims 15-17, 19, 20, 21, 22, 23, 40, 43, 44, and 45 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen and Oh in view of Stenerson. Claims 15-17, 19, and 20-23 are patentable over the cited art for reasons similar to those provided above with respect to claims 2 and 13. Claims 40 and 43-45 are patentable over the cited art for reasons similar to those provided above with respect to claim 38.

Further with respect to claim 19, the cited art fails to teach or suggest computing a first correction term using at least one of the Galois field multiply accumulators, the first correction term being equal to a first one of the syndromes; computing a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes; and computing a third correction term using at least one of the Galois field multiply accumulators, the third correction term being based in part on coefficients of at least one of the minimum-degree polynomials.

The Examiner cites Stenerson as teaching "the first correction term being equal to a first one of the syndromes." However, the cited portions of Stenerson simply recite: "Assuming one error at location j, the error value ej in relation to each syndrome is, from Equation (14): S_{127} = ejâ^{127j}," Stenerson, col. 9, lines 44-46; and "The Galois field products from the multiplier 124 (in

the form of a PROM programmed as shown in FIGS. 18C and 18D corresponding to multiplying by ff, the coefficient of the fourth term of the polynomial) are summed by exclusive-ORs 132 with the corresponding outputs of the latches 130," Stenerson, col. 18, lines 28-33. These portions of Stenerson appear to be unrelated to the calculation of a first correction term, as recited in claim 19. Neither these portions of Stenerson nor any other cited portion of any of the other references, alone or in combination, teaches or suggests "the first correction term being equal to a first one of the syndromes." Thus, for at least this reason, claim 19 is patentable over the cited art.

Claim 41 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen and Oh in view of Wolf (U.S. Pat. No. 6,385,751) (hereinafter referred to as "Wolf"). This claim is patentable over the cited art for at least the foregoing reasons provided above with respect to claim 38.

Claims 46-47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen and Oh in view of Maki et al (U.S. Pat. No. 4,873,688) (hereinafter referred to as "Maki"). These claims are patentable over the cited art for at least the foregoing reasons provided above with respect to claim 38.

Claim 48 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Alvarez et al (U.S. Patent Pub. 2002/0165962) (hereinafter referred to as "Alvarez") in view of Oh. Applicant respectfully traverses this rejection.

With respect to amended claim 48, the cited art fails to teach or suggest an OC-192 input/output card comprising: four OC-48 processors; and an OC-192 front-end application-specific integrated circuit (ASIC) connected to said four OC-48 processors, said OC-192 front-end ASIC having means for de-interleaving an OC-192 signal to create four OC-48 signals, and means for decoding error-correction codes embedded in each of the four OC-48 signalssaid decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles, wherein said decoding means uses a non-iterative algorithm to generate the error polynomial. In particular, neither Alvarez nor Oh, alone or in combination, teach or suggest using a non-iterative algorithm to generate an error polynomial. Alvarez does not provide any teachings regarding the generation of an error polynomial. Oh discloses an iterative technique for generating an error polynomial. Oh, Abstract. Thus, the references, both alone and in combination, fail to teach or suggest a

"decoding means" that "uses a non-iterative algorithm to generate the error polynomial," as recited in amended claim 48.

Additionally, there is no suggestion to combine Alvarez and Oh. "To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed combination or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references... [S]implicity and hindsight are not the proper criteria for resolving the issue of obviousness." *Ex Parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Int'f 1985). There is no mention of decoding error-correction codes in Alvarez, nor is any need for such error-correction codes mentioned. Similarly, Oh does not suggest that the error correction techniques taught in Oh would be useful in the particular system taught in Alvarez. The stated reason for the combination of the references is that "one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the time required to determine the locations of errors in the code word." Office Action, page 19. However, given that there is no mention of code words in Alvarez, let alone a mention of a need to reduce the time required to determine error locations, this statement does no appear to correspond to the teachings of the cited art. Accordingly, Applicant respectfully requests the withdrawal of this rejection.

Claims 49-50 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Alvarez and Oh in view of Stenerson. These claims are patentable over the cited art for at least the foregoing reasons provided above with respect to claim 48.

Claims 51-53 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Alvarez, Oh, and Stenerson in view of Shen. These claims are patentable over the cited art for at least the foregoing reasons provided above with respect to claim 48.

Claim 54 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Alvarez and Oh in view of Shen. This claim is patentable over the cited art for at least the foregoing reasons provided above with respect to claim 48.

Added Claim

New claim 55 is patentable by virtue of its dependence upon allowable claim 1. Furthermore, the cited art fails to teach or suggest extracting an error polynomial "using a non-iterative algorithm," as recited in claim 55. For example, as noted above, Oh explicitly states that an iterative technique is used to generate an error locator polynomial. Thus, claim 55 is additionally patentable over the cited art for at least this reason. Oh, Abstract.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5087.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on Nov 3, 2004.

Brenna A Brock — Attorney for Applicants

11/3/2004 — Date of Signature

Respectfully submitted,

Brenna A. Brock
Attorney for Applicant(s)
Reg. No. 48,509
Telephone: (512) 439-5087
Facsimile: (512) 439-5099